REMARKS

Claims 1-10 and 12-28, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-3, 7-10, 14-17, 21-24, and 28 stand rejected under 35 U.S.C. §102(b) as being anticipated by Waite (U.S. Patent No. 5,157,664). Claims 1-10 and 12-28 stand rejected under 35 U.S.C. §102(e) as being anticipated by Zorian, et al. (U.S. Patent No. 7,127,647), hereinafter referred to as Zorian. Claims 4-6, 12-13, 18-20, and 25-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Waite, in view of Bartlett, et al. (U.S. Patent No. 3,761,882), hereinafter referred to as Bartlett. Applicants respectfully traverse these rejections based on the following discussion.

The present invention teaches a method and apparatus for continuously and autonomously self-monitoring and self-adjusting the operation of an integrated circuit device (see abstract). According to paragraph [0016] of the present application, published in U.S. Patent Application Publication No. US2005/0188289, the integrated circuit device structure 100 is designed to enable on-chip performance self-testing, self-evaluation (i.e., evaluating whether the results of self-testing are within acceptable limits), and self-adjustment (i.e., self-adjusting parameters until the self-testing results are within acceptable limits).

A. Rejection Of Independent Claims 1 and 15 Based On Waite.

Wait teaches a system for testing all of the individual devices on any wafer held by a prober component of the system. Specifically, referring to col. 3, lines 31-68, Waite teaches in

Figure 1 a test and analysis system 10, and in Figure 2 similar test and analysis system 15, which includes the same features as system 10 and further incorporates an analysis subsystem 20. The system 10 uses a separate prober unit 12 that can house a wafer and that can provide the interface between the subcomponents of the tester and the individual devices that are on the wafer and that are to be tested. As discussed at col. 5, lines 55-60, the system 10 can be used to test an entire wafer containing over 300 devices in approximately 7 minutes.

Thus, the Applicants respectfully submit that Waite does not teach or suggest the "autonomously self-monitoring and self-correcting integrated circuit device" of independent claim 1 or the method of "continuously and autonomously self-monitoring and self-adjusting the operation of an integrated circuit device" of independent claim 15. Page 2 of the Office Action indicates that the preamble of claims 1 and 15 should not be accorded patentable weight. The Applicants respectfully disagree.

MPEP§ 2111.02 provides that "the determination of whether a preamble limits a claim is made on a case-by-case basis in light of the facts in each case; there is no litmus test defining when a preamble limits the scope of a claim" (see *Catalina Mktg. Int'l v. Coolsavings.com, Inc.*, 289 F.3d 801, 808, 62 USPQ2d 1781, 1785 (Fed. Cir. 2002). MPEP§211.02 further indicates that "[a] claim preamble has the import that the claim as a whole suggests for it" (see *Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620, 34 USPQ2d 1816, 1820 (Fed. Cir. 1995)) and that "[i]f the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the

balance of the claim" (see *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165-66 (Fed. Cir. 1999)).

The preamble of claim 1, "An autonomously self-monitoring and self-correcting integrated circuit device" describes a feature of the claimed integrated circuit device itself and not the intended use of that claimed integrated circuit device. As explained throughout the specification, the intended use of the integrated circuit device is to the performance of some function. The inventive aspect lies is the fact that the integrated circuit device, which performs a function, has the ability to recognize when that performance begins to degrade (i.e., is self-monitoring) and can make appropriate changes to compensate for that performance degradation (i.e., is self-correct) (see paragraph [0022] of the specification). Looking at the preamble in light of the claim as a whole, the Applicants submit that this "self-monitoring" and "self-correcting" language give meaning to (i.e., explain or further clarify) the structural features of "a self-testing controller adapted to periodically perform on-chip performance testing of said integrated circuit device" and "a processor adapted to adjust parameters of said integrated circuit device." That is, the preamble makes it known that the subject matter defined by the claims is comprise as an autonomously self-monitoring and self-correcting integrated circuit (see *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Additionally, the preamble of claim 15, "A method of continuously and autonomously self-monitoring and self-adjusting the operation of an integrated circuit device throughout the useful life of said integrated circuit device" does not merely recite the purpose of a process

without dependence thereon by features in the body of the claim. That is, the process steps of claim 15 do not stand alone, rather each claimed feature depends from the preamble.

Furthermore, MPEP 2111.02 provides that "[d]uring examination, statements in the preamble reciting the purpose or intended use of the claimed invention must be evaluated to determine whether the recited purpose or intended use results in a structural difference (or, in the case of process claims, manipulative difference) between the claimed invention and the prior art. If so, the recitation serves to limit the claim. See, e.g., *In re Otto*, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963). The Applicants submit that the preambles of structure and method claims 1 and 15 provide such structural and manipulative differences, respectively, when compared to Waite. The Office Action indicates that Figure 1, #10 of Waite disclose the various elements in the preambles of claims 1 and 15. The Applicant's respectfully disagree. Figure 1, #10, refers to an entire test and analysis system which uses a discrete prober unit (e.g., Electroglas, Inc. model EG 2010) to house a wafer containing many devices and to provide an interface between a tester subsystem 16 (e.g., model colt IIIA) and individual devices on the wafer. Those skilled in the art will recognize that a wafer prober is a machine used to load and unload wafers from their carriers and to align them with a probe card. The prober model cited by Waite was an automated prober developed by Electroglass in the early 1980's and used a robotic material handler for more efficient wafer handling (see http://www.electroglas.com/company/history.shtml). Thus, the testing system 10 is not an autonomously self-monitoring and self-correcting integrated circuit device, but rather a system to test wafers. In other words, the language in the preamble results in a structural difference (or, in

the case of process claims, manipulative difference) between the claimed invention and Waite and should be accorded patentable weight.

Additionally, the Applicants submit that Waite does not teach or suggest the following features of independent claim 1 or the similar features in amended independent claims 15: (1) "a self-testing controller adapted to periodically perform on-chip performance self-testing of said integrated circuit device;" (2) "wherein said performance self-testing comprises application of functional test sequences until failure"; and (3) "a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits."

The Office Action further provides that Waite discloses "a self-testing controller (Figure 2#22, column 5, lines 15-21) adapted to periodically perform performance self-testing on said integrated circuit device." The Applicant's respectfully disagree. As discussed above, the test system 10 of Waite is a separate and distinct system that uses probers to house and test wafers. As illustrated in Figure 2, item 22 is a component of item 10. Per col. 3, lines 60-68, the analysis subsystem 20 of system 15 generates repair and analysis information which can be transferred to a microcomputer (item 22 of Figure 2) via interfacing hardware. The cited portion of Waite (i.e., col. 5, lines 14-21) provides "One feature of the invention is recognition that the speed of the test and analysis process is severely limited by the prior art serial test and analysis sequence which has utilized a single microprocessor to perform control functions as well as computation tasks related to scanning the fail memory and determining which lines should be replaced." Thus, tester system 10 of Figure 2 incorporates the analysis subsystem 20 to allow the tester subsystem 16 to operate on one device (wafer) and the analysis subsystem 20 to analyze data formerly

collected by the tester subsystem 16 on another device (wafer) (see col. 5, lines 45-50). Nowhere in Waite is "self-testing" performed by an integrated circuit on itself. That is, nowhere in Waite is a "self-testing" controller disclosed as a component of an integrated circuit device or, more specifically, an integrated circuit component that is adapted to periodically perform on-chip performance self-testing of the integrated circuit itself.

The Office Action provides that Waite discloses "a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 1 #42)." The Applicants respectfully disagree. Per col. 5, lines 52-59, item 42 of Figure 1 refers to comparator circuitry in the tester subsystem 16 that looks at differences between the read data from the device under test to expected data and makes a pass-fail decision. That is, the compare circuitry of Waite is a component of a separate and independent testing system 10 for testing wafers, not as a component of an integrated circuit that is adapted to perform self-testing. Nowhere in Waite does it teach or suggest a comparator that is a component of an integrated circuit or, more specifically, an integrated circuit component that is adapted to evaluate whether results from on-chip self-testing (i.e., testing performed on the integrated circuit by the integrated circuit) are within acceptable limits.

The Office Action provides that Waite discloses "a processor adapted to permanently (once fuse is blown or activated for redundant columns or rows) adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (column 2, lines 60-67)." The Applicants respectfully disagree. Col. 2, lines 60-67, of Waite provides "The tester subsystem is operable in conjunction with a probe unit to write a test pattern to the memory device under test and read binary values store in the memory device. Comparator

circuitry is coupled to the tester subsystem to provide information identifying defective cells in the memory device based on differences between the test pattern and binary values read from the memory device. A fail memory stores the output of the comparator circuitry."

Nowhere in Waite does it teach or disclose adjusting the integrated circuit parameters until the results are within acceptable limits. Rather defective cells are identified in the comparator circuitry and a fail memory stores the output of the comparator circuitry. Col. 5, lines 38-50, provides that analysis system 20 can develop and output a repair scheme to a repair system for subsequent implementation. Thus, the system 10 of Waite performs a pass/fail analysis, but does not also perform the necessary repair. Nowhere in Waite does it teach or suggest a processor as a component of an integrated circuit or, more specifically, an integrated circuit component that is adapted to adjust parameters of the integrated circuit itself until the results of self-testing are evaluated by the integrated circuit and determined to be within acceptable limits.

Therefore, amended independent claims 1 and 15 are patentable over Waite. Further, dependent claims 2-7 and 16-21 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

B. Rejection Of Independent Claims 1, 8, 15 And 22 Based On Zorian.

Zorian teaches a method and system that allows for both factory and field operation tests and repair (see col. 4, line 55). Factory repair takes place during wafer probe (col. 4, line 56). Field test and repair uses a test and repair function residing on a processor to make repairs after product deployment (see col. 4, lines 57-59). In the field memory instances are tested and repaired each time the end product powers up (col. 4, lines 66-67). During field testing, the processor determines defective memory locations and, during field repair, redundant resources are allocated (col. 5, lines 0-5). Specifically, the built-in self test (BIST) engine performs tests design to detect defects in memories and a built-in self diagnosis (BISD) engine determines a location of the memory defects (see col. 5, lines 20-25). A built-in redundancy allocation (BIRA) engine then allocates available redundant rows and redundant columns in the memory array (see col. 5, lines 25-30). The "repair" refers to the fact that redundant rows and redundant columns substitute for defective components in a memory (see col. 6, lines 45-55).

The Applicants submit that Zorian does not teach or suggest the "autonomously self-monitoring and self-correcting integrated circuit device" of independent claims 1 and 8 or the method of "continuously and autonomously self-monitoring and self-adjusting the operation of an integrated circuit device" of independent claims 15 and 22. More specifically, the Applicants submit that Zorian does not teach or suggest the following features of independent claim 1 or the similar features in independent claims 8, 15 and 22: (1) "a self-testing controller adapted to periodically perform on-chip performance self-testing of said integrated circuit device, wherein said performance self-testing comprises application of functional test sequences until failure;"

and (2) "a processor adapted to adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits." The cited prior art reference also does not teach or suggest the feature in independent claims 8 and 22 indicating that the parameters are permanently adjusted "by altering the voltage supplied to portions of said integrated circuit device".

The Office Actions provides that Zorian discloses "a self-testing controller (Figure 3 "BIST") adapted to periodically perform performance self-testing on said integrated circuit device (column 5, lines 5-25)." The Applicants respectfully disagree. Those skilled in the art will recognize that there is a distinct difference between operational and performance testing of integrated circuits. That is, operational testing of integrated circuits generally involves the evaluation of the circuit or components of the circuit in their operational environment. Contrarily, performance testing specifically involves functional testing conducted in order to evaluate the compliance of the integrated circuit with specified performance requirements. The Applicants submit that the self-testing referred to in Zorian is operational testing; whereas the testing in present invention is performance testing. Specifically, the cited portion of Zorian discloses a BIST engine that "performs tests, e.g., foundry-specific test algorithms, designed to detect defects in the memories." More specifically, col. 5, lines 45-55, of Zorian details how the BIST engine runs test programs to detect faults in a memory array and the BISD engine determines the location (i.e., address) in the memory array of the defect. Such, fault detection testing is, by definition, operational testing and not performance testing (as claimed).

The Office Action further provides that Zorian discloses "a processor adapted to permanently (once a fuse is blown or activated for redundant columns or rows) adjust parameters

of said integrated circuit device until said results from said self-testing are within said acceptable limits (column 7, lines 20-45)". The Applicants respectfully disagree.

Col. 7, lines 20-45, of Zorian discusses the built-in redundancy allocation (BIRA) engine. As discussed above, after a BIST engine detects a defect in a memory cell and after a BISD engine locates that defect, the BIRA engine determines the availability of redundant components (i.e., redundant rows or columns) that can be used to substitute for the defective cell (i.e., that can be used to repair the memory). The Applicants submit that the process of substituting redundant rows or columns in a memory array for a faulting memory cell is not the same thing as "adjusting parameters of the integrated circuit until said results from said self-testing are within said acceptable limits". Specifically, in Zorian, if a memory cell of a memory array fails during operational testing, the memory cell is simply substituted with redundant components. Contrarily, in the present invention, if the integrated circuit fails performance self-testing, a processor within the integrated circuit will adjust the parameters of the integrated circuit until the results of continued self-testing are within acceptable limits. Nowhere in Zorian does it teach or disclose that the parameters of the memory array itself are adjusted until the memory array performs within acceptable limits.

The Office Action further provides that Zorian discloses "wherein said processor adjusts said parameters by altering the voltage supplied to portions of said integrated circuit by using voltage regulators (column 4, lines 50-65)." The Applicants respectfully disagree. As discussed above, the Applicants submit that Zorian does not disclose adjusting the parameters of an integrated circuit device. Furthermore, the cited portions of Zorian do not teach or suggest altering the voltage supplied to portions of the integrated circuit using voltage regulators, much

less that this is done to adjust the parameters of the integrated circuit device. Col. 4, lines 45-55, of Zorian summarizes the factory testing and repair portion (i.e., the external testing and repair portions) of that invention as well as the field testing and repair portions (i.e., self-testing and repair portions) of the invention. For example, in Zorian, the factory test includes logic testing and, if applicable, coordination of fuse box programming. More specifically, in Zorian, factory repair takes place during wafer probe in the factory, using the laser programmed fuse box. During factory repair, the wafer is subjected to a variety of stringent conditions to insure high memory instance and SoC reliability during extended voltage, temperature and frequency conditions. On the other hand, field repair uses a test and repair function residing in the processor to make repairs after product deployment. Nothing in the cited portion of Zorian discusses "altering the voltage supplied to portions of the integrated circuit device", much less doing so "until said results from said self-testing are within said acceptable limits."

Therefore, amended independent claims 1, 8, 15 and 22 are patentable over Zorian. Further, dependent claims 2-7, 9-10, 12-14, 16-21 and 23-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. Thus, Applicants submit that claims 1-10 and 12-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims and to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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/Pamela M. Riley/
Pamela M. Riley
Registration No. 40,146

Gibb & Rahman, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-0227
Fax: (301) 261-8825
Customer Number: 29154